UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/822,848	04/13/2004	Hajime Kimura	0756-7292	3205

31780 7590 12/08/2008

ERIC ROBINSON
PMB 955
21010 SOUTHBANK ST.
POTOMAC FALLS, VA 20165

EXAMINER	
XIAO, KE	

ART UNIT	PAPER NUMBER
2629	

MAIL DATE	DELIVERY MODE
12/08/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/822,848	KIMURA, HAJIME	
	Examiner	Art Unit	
	Ke Xiao	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-130* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-130* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/16/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-61 and 68-130 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiyou (JP 11-125841) in view of Kubota (US 7,196,699).

Regarding **Claims 1-7 and 100-103**, Chiyou teaches a semiconductor device (Chiyou, Fig. 1) comprising:

a pixel portion comprising a plurality of pixels (Chiyou, Fig. 10 display and sensing portion);

a first circuit (Chiyou, Fig. 10 all shift registers that are part of the drivers are considered the first circuit); and

wherein each of the plurality of pixels comprises a sensor potion and a liquid crystal element portion (Chiyou, Fig. 10 elements 1001 and 1002),

wherein the sensor portion comprises a first TFT, and the liquid crystal element portion comprises a second TFT (Chiyou, Fig. 10 elements 1003 and T1-T3 note LC elements are broadly interpreted to be light emitting elements as well),

wherein the first circuit comprises a first logical circuit and a second logical circuit (Chiyou, Fig. 10 elements 1009 and 1011);

wherein the gate of the first TFT is electrically connected to the first logical circuit and a gate of the second TFT is electrically connected to the second logical circuit (Chiyou, Fig. 10 1009 is connected to T1-T3 and 1011 is connected to 1003),

wherein the first circuit is configured to output a timing signal to the first logical circuit and the second logical circuit (Chiyou, Fig. 10 clocks are output by the universal controller to all the drivers),

wherein the second logical circuit is so configured that either one of the first logical circuit and the second logical circuit outputs a pulse signal based on the timing signal to the pixel portion (Chiyou, Fig. 10 the LCD elements and the photodiode elements are operated completely independently of each other therefore the second logical circuit 1008-1011 selects them individually), and

wherein the pulse signal output from the first logical circuit is different from the pulse signal output from the second logical circuit (Chiyou, Fig. 10 the pulses coming out of 1009 are clearly different from the pulses coming out of 1011), and

wherein when one of the first logical circuit and the second logical circuit outputs a non-selection signal to one of the first TFt and the second TFT, the other of the first logical circuit and the second logical circuit outputs a selection signal based on the timing signal to the other of the first TFT and the second TFT (Chiyou, Fig. 10 clearly the display and sensory portions are operated completely independently from each other, so they can either operate simultaneously *or* interchangeably or one without the other which mean a non-selection signal to one and a selection signal to the other).

Chiyou fails to teach a second circuit as claimed. But instead teaches a shift register which directly outputs pulses to the display electrodes. Kubota teaches a second circuit located after the shift registers in a display driver which outputs pulses to the display electrodes (Kubota, Fig. 75). It can be driven to operate using the same pulse timing as a generic shift register. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the specialized shift register and switching section of Kubota instead of the generic shift registers of Chiyou in order to reduce power consumption.

Regarding **Claims 8-31, 104-111**, Chiyou in view of Kubota further teaches that the use of NAND, AND, NOR or OR gates as switching devices for outputs to the shift registers (Kubota, Fig. 75).

Regarding **Claims 32-37**, Chiyou in view of Kubota further teaches:

wherein the first logical circuit is electrically connected to the first TFT through a first signal line (Chiyou, Fig. 10 driving gate lines),

wherein the second logical circuit is electrically connected to the second TFT through a second signal line (Chiyou, Fig. 10 sensing gate lines), and

that the first signal line can be any one of a selection signal line, a reset signal line, and a liquid crystal selection signal line, and the second signal line can be any one of a sensor selection signal line and a sensor reset line (Chiyou, Fig. 10 driving gate lines are considered selection, reset and liquid crystal selection lines, sensing gate lines are sensor selection and sensor reset lines).

Regarding **Claims 38-41 and 46-49**, Chiyou further teaches that the first TFT can be any one of a selection TFT, and a liquid crystal selection TFT, and the second TFT can be any one of a sensor selection, sensor reset TFT (Chiyou, Fig. 3 element 1003 and T1-T3).

Regarding **Claims 42-45**, Chiyou teaches wherein the other TFT is a sensor reset TFT or a sensor selection TFT (Chiyou, Fig. 3 elements T1-T3). Chiyou fails to teach a reset TFT as claimed. The examiner takes official notice that the selection TFT of a active matrix LCD selection TFT can also be used as a blanking/reset TFT. It would have been obvious to utilize the first TFT of Chiyou as a reset TFT in order to improve contrast ratio and reduce ghosting.

Regarding **Claims 50-61 and 112-115**, Chiyou in view of Kubota teaches a specialized shift register circuit with a switching section wherein the output terminals of all switching circuits are electrically connected to at least one inverter circuit (Kubota, Fig. 75).

Regarding **Claims 68-71**, Chiyou in view of Kubota teaches wherein each of the plurality of pixels comprises a liquid crystal element, a liquid crystal selection TFT, a photoelectric conversion element, a sensor selection TFT, a sensor driver TFT, and a sensor reset TFT (Chiyou, Fig. 10 elements 1001, 1002, 1003 and T1-T3).

Regarding **Claims 72-78**, Chiyou teaches that each pixel comprises one light emitting element and one photoelectric conversion element (Chiyou, Fig. 10 elements 1001 and 1002). Chiyou fails to teach that each pixel comprises three light emitting elements. The examiner takes official notice that it is well known in the art to use three

light emitting elements in a single pixel for the purposes of color reproduction, specifically red green and blue subpixels. It would have been obvious to one of ordinary skill in the art at the time of the invention to have three light emitting elements instead of one as taught by Chiyou in order to easily produce a color image.

Regarding **Claims 79-85, 116 and 117**, Chiyou further teaches a display device using the above claimed semiconductor device (Chiyou, Fig. 11 displays).

Regarding **Claims 86-92, 118 and 119**, Chiyou further teaches that the semiconductor device can be also be used as a scanner (Chiyou, Fig. 11 cameras).

Regarding **Claims 93-99, 120 and 121**, Chiyou further teaches a portable information terminal using the above claimed semiconductor device (Chiyou, Fig. 11 camera and cell phones).

Regarding **Claims 122-130**, Chiyou further teaches that the first circuit comprises shift register (Chiyou, Fig. 3 all drivers have shift registers).

Claims 62-67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiyou (JP 11-125841) in view of Kubota (US 7,196,699) as applied to Claims 1-61 and 68-130 above, and further in view of Nishigaki (US 6,246,180).

Regarding **Claims 62-67**, Chiyou in view of Kubota teaches wherein each of the plurality of pixels comprises a light emitting element, a driver TFT, a photoelectric conversion element, a sensor selection TFT, a sensor driver TFT, and a sensor reset TFT (Chiyou, Fig. 10 elements 1001, 1002, 1003 and T1-T3). Chiyou in view of Kubota fails to teach a selection TFT and a reset TFT as claimed. Nishigaki teaches an LED

type matrix display which uses a selection TFT, a driver TFT and a reset TFT in order to drive the LED it would have been obvious to replace the LCD display structure of Chiyou with the LED display structure of Nishigaki because they are interchangeable types of matrix displays and LED displays provide better power consumption characteristics and higher contrast than LCD displays.

Response to Arguments

Applicant's arguments with respect to claims 1-130 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ke Xiao whose telephone number is (571)272-7776. The examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sumati Lefkowitz/
Supervisory Patent Examiner, Art Unit 2629

/Ke Xiao/
Examiner, Art Unit 2629